## Attorney Docket No. 0756-2288 IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Shunpei YAMAZAKI

Serial No. 09/832,844

Filed: April 12, 2001

For: ELECTRO-OPTICAL DEVICE

Group Art Unit: 2826

Examiner: M. Tran

US PATENT & ITELESCAPIC OFFICE

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Attn: Finance Division

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#### REQUEST FOR REFUND

Honorable Commissioner of Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Applicants respectfully request a refund in connection with the above-identified patent application.

Applicants submitted an Information Disclosure Statement on September 21, 2005, along with a Request for Continued Examination. In light of the Request for Continued Examination, a fee is not required, therefore Applicant is entitled to a refund.

It is respectfully requested that the payment for the Information Disclosure Statement in the amount of \$180.00 be credited to Deposit Account No. 50-2280 (0756-2288). Should any additional information be needed, please do not hesitate to contact Applicants' undersigned representative at the number listed below.

Respectfully submitted,

Eric J. Robinson Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C. PMB 955 21010 Southbank Street Potomac Falls, Virginia 20165 (571) 434-6789





# **Deposit Account Statement**

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Requested Statement Month:

September 2005

**Deposit Account Number:** 

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### INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner of Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing information known to Applicant and requests that this information be made of record in the above identified application. Copies are submitted herewith in accordance with 37 C.F.R. 1.98(a).

The cited references were submitted to the Japanese Patent Office in connection with the features of "the analog switch" and "the CMOS transmission gate." In particular, the Semiconductor Handbook, <u>Basic Circuit of Analog Switch</u>, describes an analog switch circuit using the CMOS transmission gate shown in Fig. 11.65(d). The analog switch circuit of Fig. 11.65(d) drives the switch consisting of Tr3 and Tr4, by providing a pair of gate pulses each of which has opposite polarity to the other. The pair of gate pulses are provided by inputting the gate input pulse to the inverter circuit consisting of Tr1 and Tr2. English translations of the drawings of the reference are shown on the copy of the reference by manuscript.

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This Information Disclosure Statement is being submitted after the issuance of an non-final Office Action, therefore, the \$180 fee is enclosed.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280. A duplicate copy of this sheet is attached.

Respectfully submitted,

Eric J. Robinson

Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C. PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789

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Approved for use through 10/31/2002. OMB 0651-0031

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ork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid QMB control number. Complete if Known 09/832,844 Application Number FORMATION DISCLOSURE April 12, 2001 Filing Date STATEMENT BY APPLICANT Shunpei YAMAZAKI First Named Inventor 2826 (use as many sheets as necessary) Group Art Unit M. Tran Examiner Name 0756-2288 Attorney Docket Number

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		H. YANAI, 3.3.2 Basic Circuit of Analog Switch, Semiconductor Handbook, 2 <sup>nd</sup> Edition, Pages 842-843, 1977.							

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